



Attorney's Docket No.: 42P16680

PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In Re Patent Application of: )  
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                                    )  
                                   Justin K. Brask et al.      )  
                                    )  
                                   Application No.: 10/750,061    )  
                                    )  
                                   Filed: December 30, 2003      )  
                                    )  
                                   For: NONPLANAR TRANSISTORS WITH  
                                     METAL GATE ELECTRODES      )  
                                    )  
                                    )

Commissioner for Patents  
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Alexandria, Virginia 22313-1450

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Teresa Mattox

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If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: February 15, 2006,

  
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<b>Examiner Signature</b>		<b>Date Considered</b>	
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(use as many sheets as necessary)

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## *Complete if Known*

Application Number	10/750,061
Filing Date	December 30, 2003
First Named Inventor:	Justin K. Brask, et al.
Art Unit	2812
Examiner Name	Lindsay Jr., Walter Lee

## NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T <sup>2</sup>
		JING GUO, et al. "Performance Projections for Ballistic Carbon Nanotube Field-Effect Transistors", Applied Physics Letters, Vol. 80, No. 17, pp. 3192-3194 (April 29, 2004)	
		ALI JAVEY, et al., "High-K Dielectrics for Advanced Carbon-Nanotube Transistors and Logic Gates", Advance Online Publication, Published online, pp. 1-6 (November 17, 2002)	
		RICHARD MARTEL, et al., "Carbon Nanotube Field Effect Transistors for Logic Applications" IBM, T.J. Watson Research Center, 2001 IEEE, IEDM 01, pp. 159-162	
		DAVID M. FRIED, et al., "High-Performance P-Type Independent-Gate FinFETs, IEEE Electron Device Letters", Vol 25, No. 4, April 2004, pp. 199-201.	
		DAVID M. FRIED, et al., "Improved Independent Gate N-Type FinFET Fabrication and Characterization", IEEE Electron Device Letters", Vol. 24, No. 9, September 2003, pp. 592-594.	
		CHARLES KUO, et al. "A Capacitorless Double Gate DRAM Technology for Sub-100-nm Embedded and Stand-Alone Memory Applications", IEEE Transactions on Electron Devices", Vol. 50, No. 12, December 2003, pp. 2408-2416.	
		CHARLES KUO, et al., "A Capacitorless Double-Gate DRAM Cell Design for High Density Applications", 2002 IEEE International Electron Devices Meeting Technical Digest, December 2002, pp. 843-846	
		TAKASHI OHSAWA, et al., "Memory Design Using a One-Transistor Gain Cell on SOI", IEEE Journal of Solid-State Circuits, Vol. 37, No. 11, November 2002, pp. 1510-1522	
		T. TANAKA, et al., "Scalability Study on a Capacitorless 1T-DRAM: From Single-Gate PD-SOI to Double-Gate FinDRAM", 2004 IEEE International Electron Devices Meeting Technical Digest, December 2004, 4 pages.	L
		T. M. MAYER, et al., "Chemical Vapor Deposition of Fluoroalkylsilane Monolayer Films for Adhesion Control in Microelectromechanical Systems" 2000 American Vacuum Society B 18(5), Sep/Oct 2000, pp. 2433-2440	
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